AMENDMENTS TO THE CLAIMS

1. (Previously Presented) Circuitry for providing external access to signals that are internal to an integrated circuit, said circuitry comprising:

a network comprising a plurality of multiplexers physically distributed throughout the integrated circuit, each of said multiplexers having its inputs coupled to a nearby set of nodes within the integrated circuit;

a trigger event generator receiving a first N bits of sampled data from said network, said trigger event generator including a definable mask and selectively performing a boolean operation on said sampled data based on said mask to provide a trigger event; and

a FIFO storage array that stores at least a portion of the sampled data.

2. (Original) The circuitry according to claim 1 wherein said trigger event generator further comprises a switch for selectively providing, as said trigger event, one of (i) a result of said boolean operation on said sampled data, (ii) a performance counter event signal, and (iii) an externally applied trigger signal.

3. (Original) The circuitry according to claim 1 further comprising a counter providing an intermediate trigger in response to a predetermined number of said trigger events.

4. (Original) The circuitry according to claim 3 further comprising a trigger delay providing a sample command a predetermined number of cycles following said intermediate trigger.

5. (Original) The circuitry according to claim 4 wherein said predetermined number of cycles represent respective operating cycles of the integrated circuit.

6. (Original) The circuitry according to claim 4 wherein said predetermined number of cycles represent respective machine clock cycles.

7. (Original) The circuitry according to claim 4 further comprising a programmable register storing a value corresponding to said predetermined number of cycles.

8. (Original) The circuitry according to claim 7 wherein said programmable register selectively increments said value corresponding to said predetermined number of cycles by a predetermined number of said cycles.

9. (Previously Presented) The circuitry according to claim 4 further comprising a sampling circuit responsive to said sample command to identify target data.

10. (Original) The circuitry according to claim 1 further comprising a trigger delay providing a sample command a predetermined number of cycles following said trigger event.

11. (Original) The circuitry according to claim 10 further comprising a sampling circuit responsive to said sample command to identify target data.

12. (Original) The circuitry according to claim 1 further comprising a sampling circuit responsive to said trigger event to identify target data.

13. (Original) The circuitry according to claim 12 wherein said target data comprises said first N bits of sampled data supplied by said network.

14. (Original) The circuitry according to claim 12 wherein said target data consists of a second N bits of sampled data supplied by said network.

15. (Original) The circuitry according to claim 12 wherein said sampling circuit includes a memory storing said target data.

16. (Original) The circuitry according to claim 12 wherein said sampling circuit includes switching circuitry configured to selectively provide a predetermined portion of said target data.

17. (Previously Presented) Circuitry for providing external access to signals that are internal to an integrated circuit, said circuitry comprising:

a network comprising a plurality of multiplexers physically distributed throughout the integrated circuit, each of said multiplexers having its inputs coupled to a nearby set of nodes within the integrated circuit;

a trigger event generator receiving a first N bits of sampled data from said network, said trigger event generator including a definable mask and selectively performing a boolean operation on said sampled data based on said mask to provide a trigger event; and

a sampling circuit responsive to said trigger event to identify target data, wherein said sampling circuit includes switching circuitry configured to selectively provide a predetermined portion of said target data, wherein said predetermined portion of said target data is N/M bits wide where N/M is a positive integer.

18. (Previously Presented) The circuitry according to claim 17 wherein said sampling circuit includes multiplexing circuitry configured to combine M of said portions of said target data into a data unit N bits wide.

19. (Previously Presented) The circuitry according to claim 12 wherein said sampling circuit includes a FIFO storage array.

20. (Previously Presented) Circuitry for providing external access to signals that are internal to an integrated circuit, said circuitry comprising:

a network comprising a plurality of multiplexers physically distributed throughout the integrated circuit, each of said multiplexers having its inputs coupled to a nearby set of nodes within the integrated circuit;

a trigger event generator receiving a first N bits of sampled data from said network, said trigger event generator including a definable mask and selectively performing a boolean operation on said sampled data based on said mask to provide a trigger event; and

a sampling circuit responsive to said trigger event to identify target data, wherein said sampling circuit includes a FIFO storage array, and wherein said FIFO storage array is N/M bits wide where N/M is a positive integer.

21. (Canceled)